In The Claims:

Please amend the claims as follows.

1. (Currently Amended) A substrate structure of Flip Chip package comprising:

a plurality of patterned circuit layers;

at least an insulative layer stacked between the patterned circuit layers for isolating the patterned circuit layers, and the patterned circuit layers are electrically connected one another, and one of the patterned circuit layer is positioned on the surface of the substrate of the flip chip package as a top patterned circuit layer, and the top patterned circuit layer comprises at least a plurality of first mounting pads and a plurality of second mounting pads; and

a solder mask layer covering the patterned circuit layer on the surface of the substrate of the flip chip package, the solder mask layer partially covering a first top surface of the first mounting pads while entirely exposing a second top surface and sidewalls of the second mounting pads, wherein the first mounting pads are disposed at a peripheral region of the substrate and the second mounting pads are disposed at a central region of the substrate, and wherein said first and second mounting pads ~~are for electrically contacting with~~ can be directly attached to corresponding bumps of a chip.

2. (Previously presented) The substrate structure of Flip Chip package of claim 1 wherein the material for the insulative layer is selected from the group consisting of flame-retardant epoxy-glass fabric composite resin, Bismaleimide-Triazine (BT), and epoxy.

3. (Original) The substrate structure of Flip Chip package of claim 1 wherein each of the patterned circuit layer is formed by a copper foil layer defined by photolithographic and etching processes.

4. (Original) The substrate structure of Flip Chip package of claim 1 wherein the pitch of the first mounting pads is smaller than the pitch of the second mounting pad.

5. (Original) The substrate structure of Flip Chip package of claim 1 wherein a plurality of vias are disposed in the insulative layer for electrically connecting to the patterned circuit layers.

Claim 6 (canceled).

7. (Currently Amended) A substrate structure of Flip Chip package comprising:

a plurality of patterned circuit layer;

at least an insulative layer stacked between the patterned circuit layers for isolating the patterned circuit layers, and the patterned circuit layers are electrically connected one another, and one of the patterned circuit layer is positioned on the surface of the substrate of the flip chip package as a top patterned circuit layer, and the top patterned circuit layer comprises at least a plurality of first mounting pads and a plurality of second mounting pads;

a solder mask layer covering the top patterned circuit layer on the surface of the substrate of the flip chip package, the solder mask layer partially covering a first top surface of the first

mounting pads while entirely exposing a second top surface and sidewalls of the second mounting pads, wherein the first mounting pads surround the second mounting pads;

a chip having an active surface with a plurality of bumps disposed thereon wherein the chip has its active surface face to the surface of the substrate of the flip chip package, and the bumps ~~are electrically contacted with~~ can be directly attached to their corresponding first bonding pads and second bonding pads respectively; and

an underfill material filling between the active surface of the chip and the top surface of the substrate of the flip chip package.

8. (Previously presented) The substrate structure of Flip Chip package of claim 7 wherein the material for the insulative layer is selected from the group consisting of flame-retardant epoxy-glass fabric composite resin, Bismaleimide-Triazine (BT), and epoxy.

9. (Original) The substrate structure of Flip Chip package of claim 7 wherein each of the patterned circuit layer is formed by a copper foil layer defined by photolithographic and etching processes.

10. (Original) The substrate structure of Flip Chip package of claim 7 wherein the pitch of the first mounting pads is smaller than the pitch of the second mounting pad.

11. (Original) The substrate structure of Flip Chip package of claim 7 wherein a plurality of vias are disposed in the insulative layer for electrically connecting to the patterned circuit layers.

12. (Original) The substrate structure of Flip Chip package of claim 7 wherein the first mounting pads are disposed on the periphery region of the substrate of the flip chip package while the second mounting pads are disposed in the central region of the substrate of the flip chip package.

13. (Original) The substrate structure of Flip Chip package of claim 7 wherein the bumps attach only to the top surface of the first mounting pads.

14. (Original) The substrate structure of Flip Chip package of claim 7 wherein the bumps attach to both the top surface and side surfaces of the second mounting pads.

Claims 15 and 16 (canceled).